

# ***THS4505EVM***

## *User's Guide*

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## EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of  $\pm 5$  V and the output voltage range of +5 V and -5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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# Read This First

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### ***About This Manual***

This manual provides information about using the THS4505 fully differential amplifier on evaluation module PCB marked with Edge # 6439396. Additionally, this document provides a good example of PCB design for high-speed applications. The user should keep in mind the following points.

- The design of the high speed amplifier PCB is a sensitive process.
- The user must approach the PCB design with care and awareness.
- It is recommended that the user initially review the data sheet of the device under test.
- It is helpful to review the schematic and layout of the THS4505EVM to determine the design techniques used in the evaluation board.
- It is recommended that the user review the application note *Fully Differential Amplifiers* (literature number SLOA054) to gain more insight about differential amplifiers. This application note reviews fully differential amps and presents calculations for various filters.

### ***How to Use This Manual***

This document contains the following chapters:

- Chapter 1—Introduction and Description
- Chapter 2—Using the THS4505EVM
- Chapter 3—THS4505EVM Applications
- Chapter 4—High-Speed Amplifier PCB Layout Tips
- Chapter 5—EVM Hardware Description

### ***Information About Cautions and Warnings***

This book may contain cautions and warnings.

**This is an example of a caution statement.**

**A caution statement describes a situation that could potentially damage your software or equipment.**

**This is an example of a warning statement.**

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### **Electrostatic Sensitive Components**



**This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, refer to SSYA008.**

### **Related Documentation From Texas Instruments**

The URLs below are correct as of the date of publication of this manual. Texas Instruments applications apologizes if they change over time.

- THS4505 data sheet (literature number SLOS350)
- Application report (literature number SLOA054), *Fully Differential Amplifiers*
- Application report (literature number SLOA069), *How (Not) to Decouple High Speed Op Amp Circuits*,  
<http://www-s.ti.com/sc/psheets/sloa069/sloa069.pdf>
- Application report (literature number SLOA072), *Single Supply Differential Op Amp Techniques*,  
<http://www-s.ti.com/sc/psheets/sloa072/sloa072.pdf>

- Application report (literature number SLMA002), *PowerPAD Thermally Enhanced Package*,  
<http://www-s.ti.com/sc/psheets/slma004/slma002.pdf>
- Application report (literature number SLMA004), PowerPAD Made Easy,  
<http://www-s.ti.com/sc/psheets/slma004/slma004.pdf>
- Application report (literature number SSYA008), Electrostatic Discharge (ESD), <http://www-s.ti.com/sc/psheets/ssya008/ssya008.pdf>

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# Introduction and Description

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The Texas Instruments THS4505 evaluation module (EVM) helps designers evaluate the performance of the THS4505 fully differential operational amplifier (FDA). Also, this EVM is a good example of high speed PCB design.

This document details the THS4505EVM. It includes a list of EVM features, a brief description of the module illustrated with a series of schematic diagrams, EVM specifications, details on connecting and using the EVM, and a discussion of high-speed amplifier design considerations.

This EVM enables the user to implement various circuits to clarify the available configurations presented by the schematic of the EVM. The user is not limited to the circuit configurations presented here. The EVM provides enough hardware hooks that the only limitation should be the creativity of the user.

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## 1.1 Description

The THS4505EVM provides a platform for developing high speed FDA application circuits. It contains the THS4505 high speed FDA, a number of passive components, and various features and footprints that enable the user to experiment, test, and verify various operational amplifier circuit implementations. The PC board measures 3.08 by 2.42 inches.

## 1.2 Evaluation Module Features

THS4505 high speed operational amplifier EVM features include:

- Wide operating supply voltage range: single supply 5 Vdc to dual supply  $\pm 5$  Vdc operation (see the device data sheet). Single supply operation is obtained by jumpering GND (J7) to  $-V_S$  (J5).
- Single-ended and fully differential input capability.
- Single-ended and fully differential output capability.
- Nominal 50- $\Omega$  input termination (R1||R2). Termination can be configured according to the application requirement.
- $V_{OCM}$  direct input through TP1.
- Output transformer T1.
- Footprints for antialiasing filter implementation using locations R6, R7, C5, and C6.
- Footprints for low pass filter implementation using locations C3, C4.
- 800- $\Omega$  load provided through R8, R10, R9, and R11 reflected through T1.
- Three convenient GND test points on the PCB.
- Power supply ripple rejection capacitors (C8 and C11).
- Decoupling capacitors (C9, C12) populated with 0.1  $\mu$ F capacitors—design final decoupling in accordance with SLOA069
- PowerPAD™ heatsinking capability.
- A good example of high-speed amplifier PCB design and layout

## 1.3 THS4505EVM Operating Conditions

- Supply voltage range,  $\pm V_S$       5 V to  $\pm 5$  V (see the device data sheet)
- Supply current,  $I_S$                       (see the device data sheet)

For complete THS4505 amplifier IC specifications, parameter measurement information, and additional application information, see the THS4505 data sheet, TI literature number SLOS350.

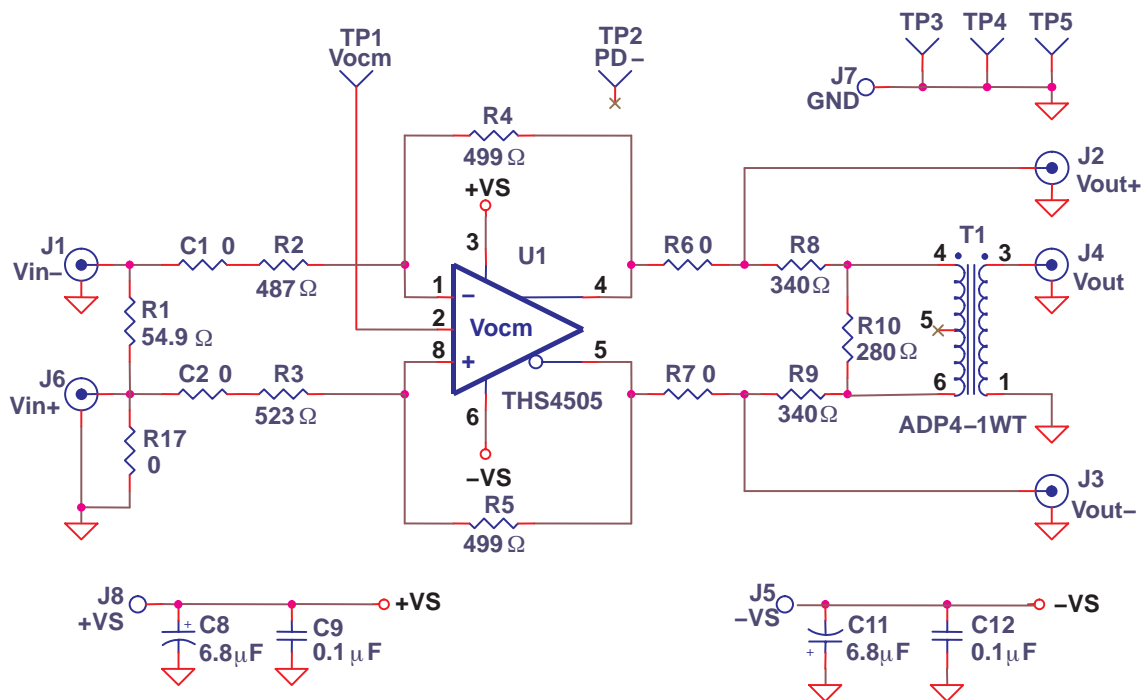
## 1.4 EVM Default Configuration

As delivered, the EVM has a fully functional example circuit; just add power supplies, a signal source, and monitoring instrument. See Figure 1–1 for the default schematic diagram. The user can change the gain by changing the ratios of the feedback and gain resistors (see the device data sheet for recommended resistor values). The complete EVM schematic in Chapter 5 shows all component locations.

The default configuration assumes a 50- $\Omega$  signal source, and contains a termination resistor R1 for the source.

Some components such as C8, C9, C11, C12, TP1, TP2, R10, T1, and J4 are omitted on the application schematics of Chapter 3 for clarity.

Figure 1–1. Schematic of the Populated Circuit on the EVM (Default Configuration)





# Using the THS4505EVM

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This section describes how to connect the THS4505EVM to test equipment. It is recommended that the user connect the EVM as described in this section to avoid damage to the EVM or the THS4505 installed on the board.

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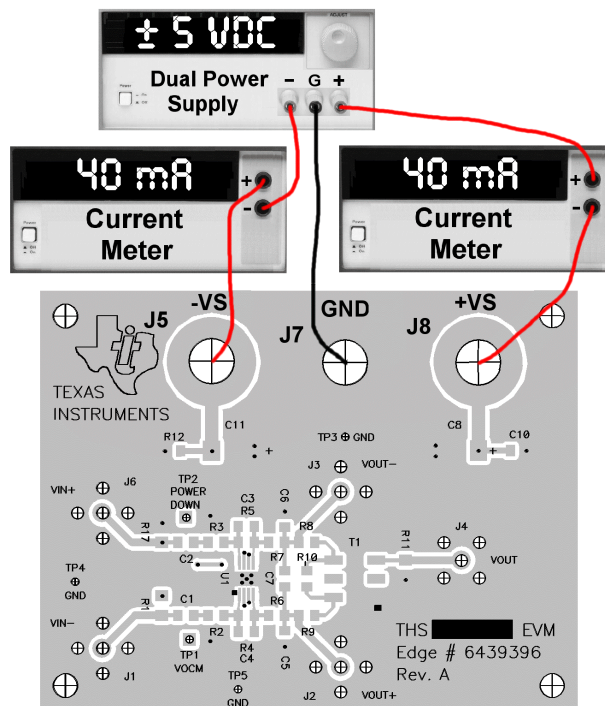
## 2.1 Required Equipment

- One dual-output dc power supply ( $\pm 5$  V, 1 A output minimum)
- Two dc current meters with resolution to 1 mA and capable of the maximum current the dc power supply can supply.
- 50- $\Omega$  source impedance function generator (1 MHz, 10 V<sub>PP</sub> sine wave)
- Oscilloscope (50-MHz bandwidth minimum, 50- $\Omega$  input impedance)
- Three BNC-to-SMA cables
- BNC-to-BNC cable
- Five banana-to-banana wires; 4 red, 1 black

## 2.2 Power Supply Connection (Refer to Figure 2–1)

- 1) Set the dual dc power supply to  $\pm 5$  V. If available, set the current limit on the dc power supply to 100 mA.
- 2) Make sure the dual dc power supply is turned off before proceeding to the next step.
- 3) Connect the positive (+) terminal of the power supply to the positive (+) terminal of the current meter number 1.
- 4) Connect the negative (-) terminal of the current meter number 1 to +VS (J8).
- 5) Connect the common ground terminal of the power supply to GND (J7).
- 6) Connect the negative (-) terminal of the power supply to the negative (-) terminal of the second current meter.
- 7) Connect the positive (+) terminal of the current meter number 2 to -VS (J5).

Figure 2–1. Power Supply Connection for  $\pm 5$  Vdc





## 2.3 Function Generator Setup

### Note:

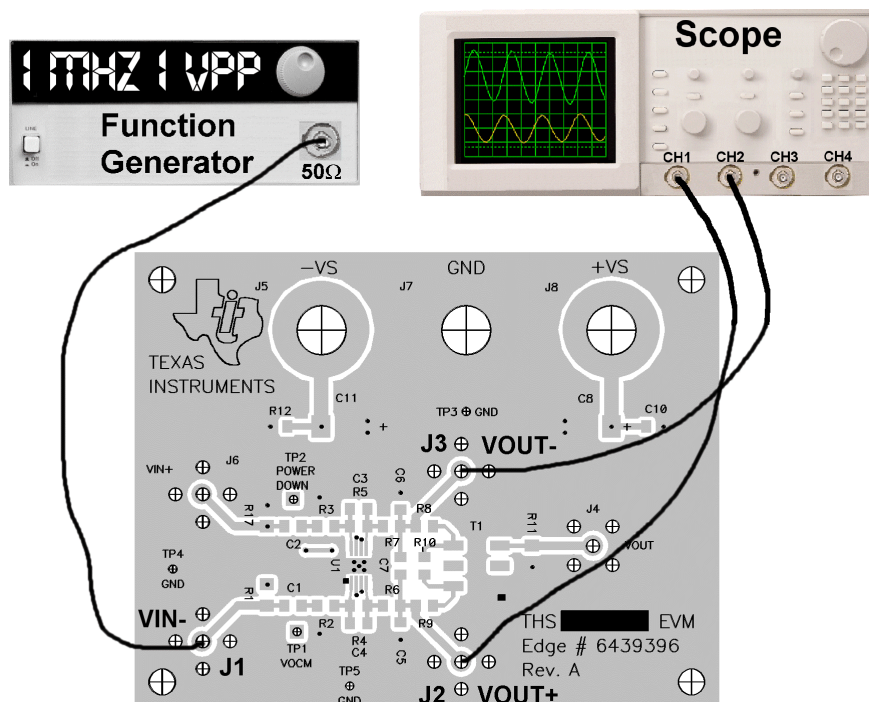
The oscilloscope channels (CH1 and CH2) must be set to 50- $\Omega$  input impedance for proper results.

- 1) Connect the function generator to oscilloscope channel 1.
- 2) Set vertical channels 1 and 2 of the oscilloscope to 0.2 V/division and the time-base to 0.1  $\mu$ s/division.
- 3) Set the function generator to generate a 1-MHz,  $\pm 0.5$  V (1 V<sub>PP</sub>) sine wave with no dc offset.
- 4) Verify that the output is 1 MHz,  $\pm 0.5$  V (1 V<sub>PP</sub>).
- 5) Disable the function generator output before proceeding to the next step.
- 6) Disconnect the cable from the oscilloscope, retaining the setting of the function generator.

## 2.4 Signal Connection V<sub>IN-</sub> (Refer to Figure 2-2)

- 1) Using a BNC-to-SMA cable, connect the function generator to J1 (VIN-).
- 2) Using a BNC-to-SMA cable, connect the oscilloscope channel 1 to J2 (VOUT+).
- 3) Using a BNC-to-SMA cable, connect the oscilloscope channel 2 to J3 (VOUT-).

Figure 2-2. Signal Connections





# **THS4505EVM Applications**

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Example applications are presented in this chapter. These applications demonstrate the most popular circuits to the user, but many other circuits can be constructed. The user is encouraged to experiment with different circuits, exploring new and creative design techniques. After all, that is the function of an evaluation board.

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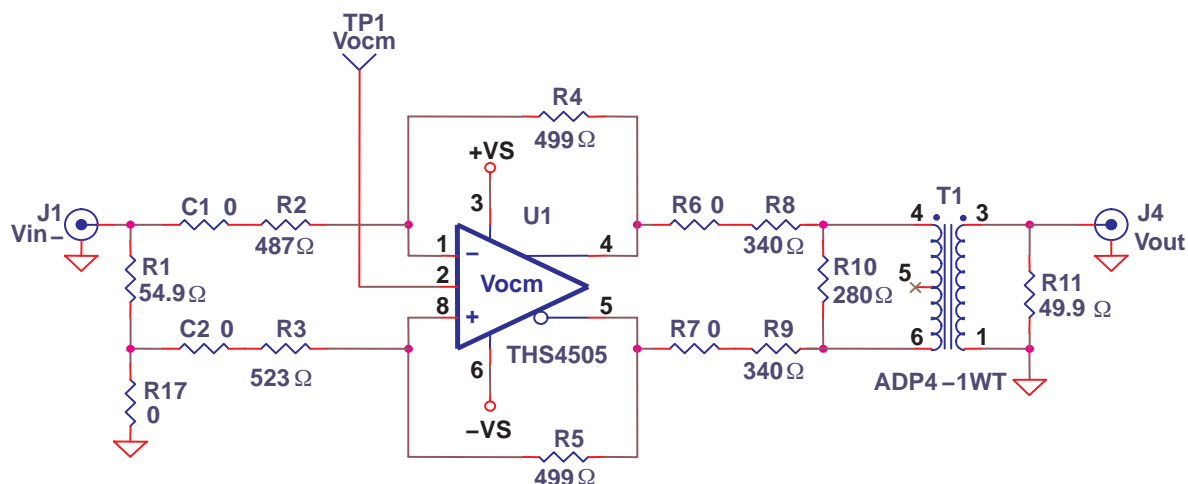
### 3.1 Single-Ended In/Single-Ended Out, Utilizing Transformer

The fully differential amp output can be monitored by a single-ended instrument at J4. The THS4505EVM utilizes Mini-Circuits CD542 footprint transformers to make the fully differential-to-single-ended conversion. An ADP4-1WT transformer is installed on the board.

R8, R9, and R10 are chosen such that the load on the fully differential amp is  $800\ \Omega$  when combined with the load impedance transformed by the turn ratio T1. This load is chosen because it is a common input impedance value for ADCs, and is the impedance at which many fully differential amp parameters are measured. The  $800\text{-}\Omega$  load occurs when one of two conditions is met:

- R11 is installed and the measuring instrument is set to  $1\text{-M}\Omega$  input impedance
- or
- R11 is not installed and the measuring instrument has an input impedance of  $50\ \Omega$ .

Figure 3–1. Single-Ended In/Single-Ended Out, Utilizing Transformer



### 3.2 Single-Ended to Fully Differential Application

Single-supply, single-ended to fully differential conversion is a popular application for fully differential amps. Until the introduction of fully differential amps such as the THS4505, it was necessary to include two coupling capacitors to prevent the input signal from violating the input common mode range of the op amp. The THS4505 is optimized for ground-referenced inputs in single supply applications—no capacitors are required.

When operated, the output voltage is offset to  $+VS/2$  ( $2.5\text{ V}$ ) by the internal action of  $V_{OCM}$ .

Figure 3–2. Single Supply Operation

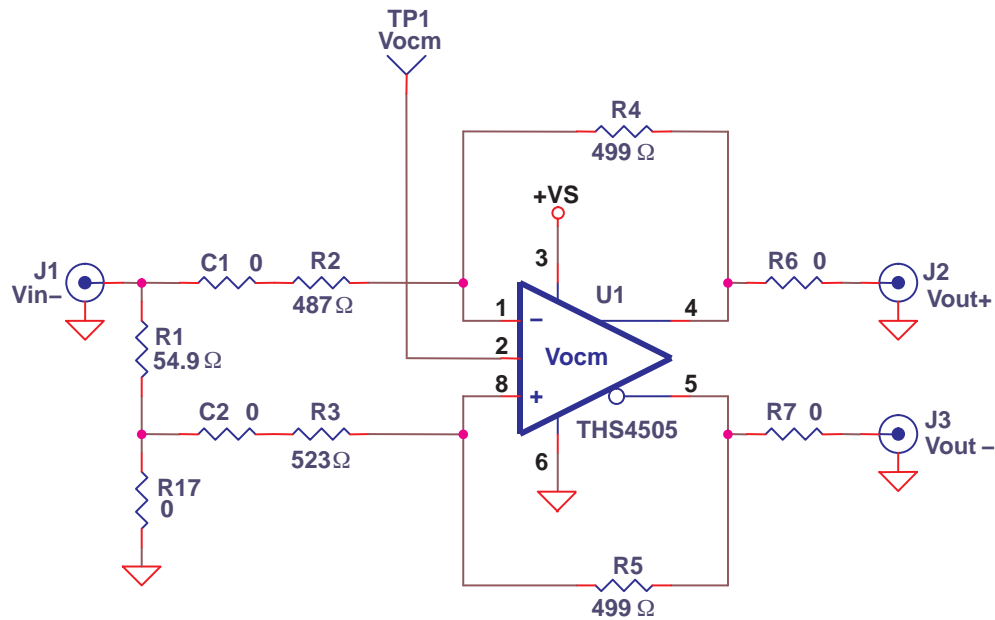
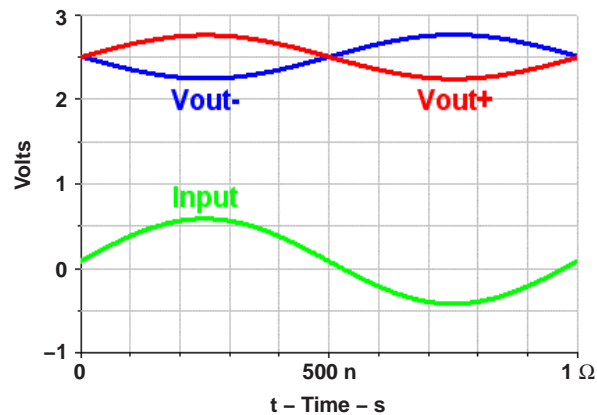


Figure 3–3. Output of a Ground Referenced, Single-Supply Application



Note that a small offset is present on the input voltage. This is caused by a voltage divider formed by  $R_2 + R_4$  and the parallel combination of  $R_1$  and the source resistance of the signal generator.

This application circuit has interaction between  $R_{\text{source}}$ ,  $R_{\text{termination}}$ , and  $R_g$ . Texas Instruments has provided an engineer design utility to facilitate the design of these circuits. Engineer design utilities are available on the *Amplifiers and Comparators* section of the *Analog and Mixed Signal* portion of the TI web page.

The designer should be aware that each individual feedback path is an inverting path. There is no *noninverting* gain circuit for fully differential amps. The designer should also be aware that the gain is affected by the open loop characteristic of the FDA, the same as single-ended op amps. If there is sufficient safety margin between the closed loop response and open loop response of the FDA (40 dB or more), the error contribution from the open loop response of the FDA is negligible and can be ignored.



# High-Speed Amplifier PCB Layout Tips

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The THS4505EVM layout has been designed for use with high-speed signals and can be used as an example when designing PCBs incorporating the THS4505. Careful attention has been given to component selection, grounding, power supply bypassing, and signal path layout. Disregarding these basic design considerations could result in less than optimum performance of the THS4505 high-speed operational amplifier. Surface-mount components are selected because of the extremely low lead inductance associated with this technology. This helps minimize both stray inductance and capacitance. Also, because surface-mount components are physically small, the layout can be very compact.

Tantalum power supply bypass capacitors at the power input pads help filter switching transients from the laboratory power supply. Power supply bypass capacitors are placed as close as possible to the IC power input pins in order to minimize the return path impedance. This improves high frequency bypassing and reduces harmonic distortion. The GND side of these capacitors should be located close to each other, minimizing the differential current loops associated with differential output currents. If poor high frequency performance is observed, replace the 0.1- $\mu$ F capacitors with microwave capacitors with a self-resonance at the frequency that produces trouble. A proper ground plane on both sides of the PCB should be used with high-speed circuit design. This provides low-inductive ground connections for return current paths.

In the area of the amplifier input pins, however, the ground plane has been removed to minimize stray capacitance and reduce ground plane noise coupling into these pins. This is especially important for the inverting input pin. As low as 1-pF capacitance at the inverting input can significantly affect the response of the amplifier or even oscillation.

In general, it is best to keep signal lines as short and as straight as possible. Incorporation of microstrip or stripline techniques is also recommended when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either 50  $\Omega$  or 75  $\Omega$ , as required by the application. Such a signal line must also be properly terminated with an appropriate resistor.

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Circuit pathways should be made as symmetrical as possible for both feedback pathways to minimize second and other even harmonic content.

The printed-circuit board that is used with PowerPAD packages must have features included in the design to remove the heat from the package efficiently. As a minimum, there must be an area of solder-tinned-copper underneath the PowerPAD package. This area is called the thermal land. The thermal land varies in size depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, this thermal land may or may not contain thermal vias depending on PCB construction. The requirements for thermal lands and thermal vias are detailed in <http://www-s.ti.com/sc/techlit/slma002> and SLMA004.

Finally, all inputs and outputs must be properly terminated, either in the layout or in the load instrumentation. Unterminated lines, such as coaxial cable, can appear to be a reactive load to the amplifier. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears to be purely resistive, and reflections are absorbed at each end of the line. Another advantage of using an output termination resistor is that capacitive loads are isolated from the amplifier output. This isolation helps minimize the reduction in the amplifier's phase-margin and improves the amplifier stability resulting in reduced peaking and settling times.



# EVM Hardware Description

This chapter describes the EVM hardware. It includes the EVM parts list, and printed-circuit board layout.

Table 5–1. THS4505EVM Bill of Materials

Item	Description	SMD Size	Reference Designator	PCB Qty.	Manufacturer's Part Number	Distributor's Part Number
1	CAP, 6.8 $\mu$ F, tanatalum, 35 V, 10%	D	C8, C11	2	(AVX) TAJD685K035R	(Garrett) TAJD685K035R
2	CAP, 0.1 $\mu$ F, ceramic, X7R, 16 V	0508	C9, C12	2	(AVX) 0508YC104KAT2A	(Garrett) 0508YC104KAT2A
3	Open	0805	C3, C4, C5, C6, C7, C10	6		
4	Open	1206	C13, C14	2		
5	Open	0805	R11, R12, R13, R14, R15, R16	6		
6	Resistor, 0 $\Omega$ , 1/8 W	0805	C1, C2, R6, R7	4	(Phycomp) 9C08052A0R00JLHFT	(Garrett) 9C08052A0R00JLHFT
7	Resistor, 280 $\Omega$ , 1/8 W, 1%	0805	R10	1	(Phycomp) 9C08052A2800FKHFT	(Garrett) 9C08052A2800FKHFT
8	Resistor, 340 $\Omega$ , 1/8 W, 1%	0805	R8, R9	2	(Phycomp) 9C08052A3400FKHFT	(Garrett) 9C08052A3400FKHFT
9	Resistor, 487 $\Omega$ , 1/8 W, 1%	0805	R2	1	(Phycomp) 9C08052A4870FKHFT	(Garrett) 9C08052A4870FKHFT
10	Resistor, 499 $\Omega$ , 1/8 W, 1%	0805	R4, R5	2	(Phycomp) 9C08052A4990FKHFT	(Garrett) 9C08052A4990FKHFT
11	Resistor, 523 $\Omega$ , 1/8 W, 1%	0805	R3	1	(Phycomp) 9C08052A5230FKHFT	(Garrett) 9C08052A5230FKHFT
12	Resistor, 0 $\Omega$ , 1/4 W	1206	R17	1	(Phycomp) 9C12063A0R00JLHFT	(Garrett) 9C12063A0R00JLHFT
13	Resistor, 54.9 $\Omega$ , 1/4 W, 1%	1206	R1	1	(Phycomp) 9C12063A54R9FKRFT	(Garrett) 9C12063A54R9FKRFT
14	Transformer, 4:1	CD542	T1	1	(Mini-Circuits) ADT4–1WT	(Mini-Circuits) ADT4–1WT
15	Test points (black)		TP3, TP4, TP5	3	(Keystone) 5001	(Allied) 839–3601
16	Test points (red)		TP1, TP2	2	(Keystone) 5000	(Allied) 839–3600

Item	Description	SMD Size	Reference Designator	PCB Qty.	Manufacturer's Part Number	Distributor's Part Number
17	Jack, banana receptacle, 0.25" diameter hole		J5, J7, J8	3	(HH Smith) 101	(Newark) 35F865
18	Connector, SMA PCB Jack		J1, J2, J3, J4, J6	5	(Amphenol) 901-144-8RFX	(Newark) 01F2208
19	Standoff, 4-40 Hex, 0.625" Length			4	(Keystone) 1804	(Allied) 839-2089
20	Screw, Phillips, 4-40, 0.250"			4	SHR-0440-016-SN	
21	IC, THS4505		U1	1	(TI) THS4505DGN	
22	Board, printed circuit			1	(TI) EDGE # 6439396	

Figure 5-1. Top Layer 1 (Signals for THS4505EVM)

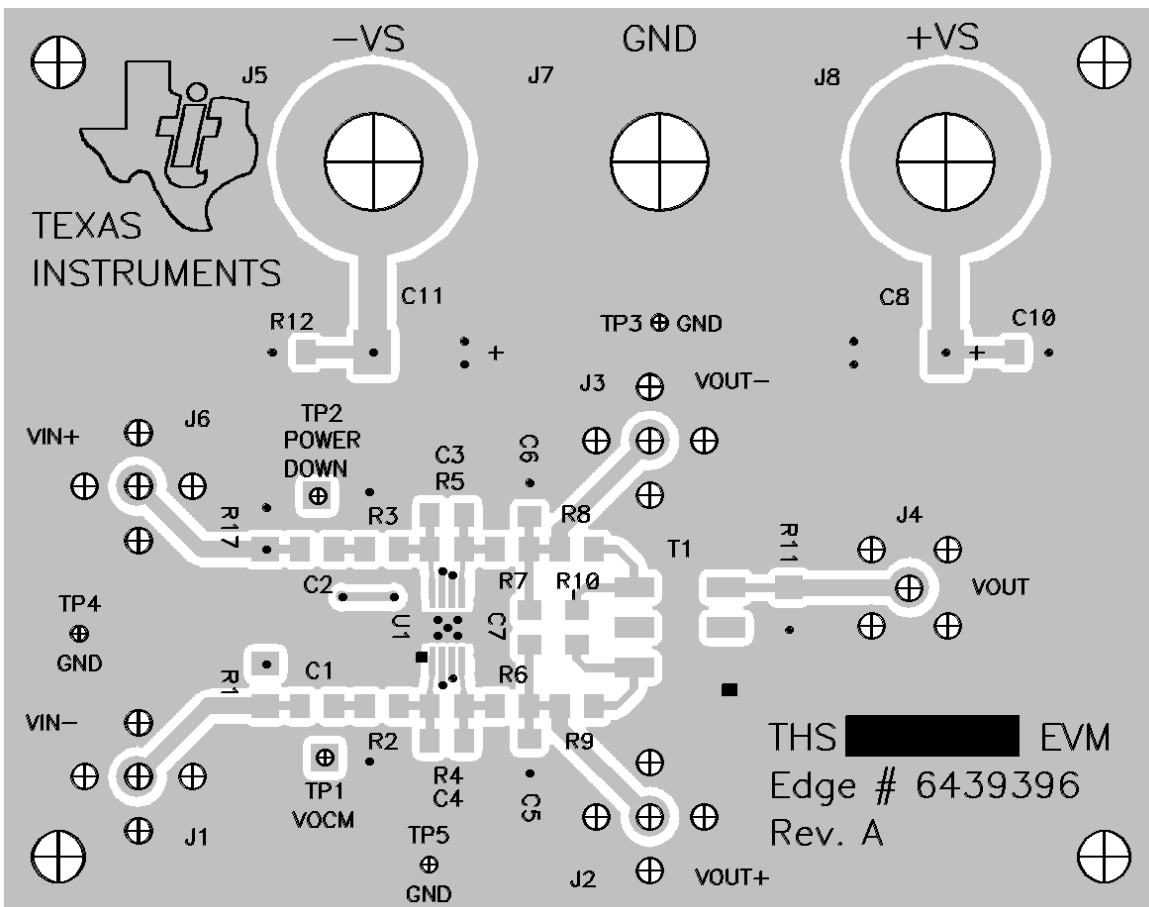


Figure 5-2. Bottom Layer 2 (Ground and Signal)

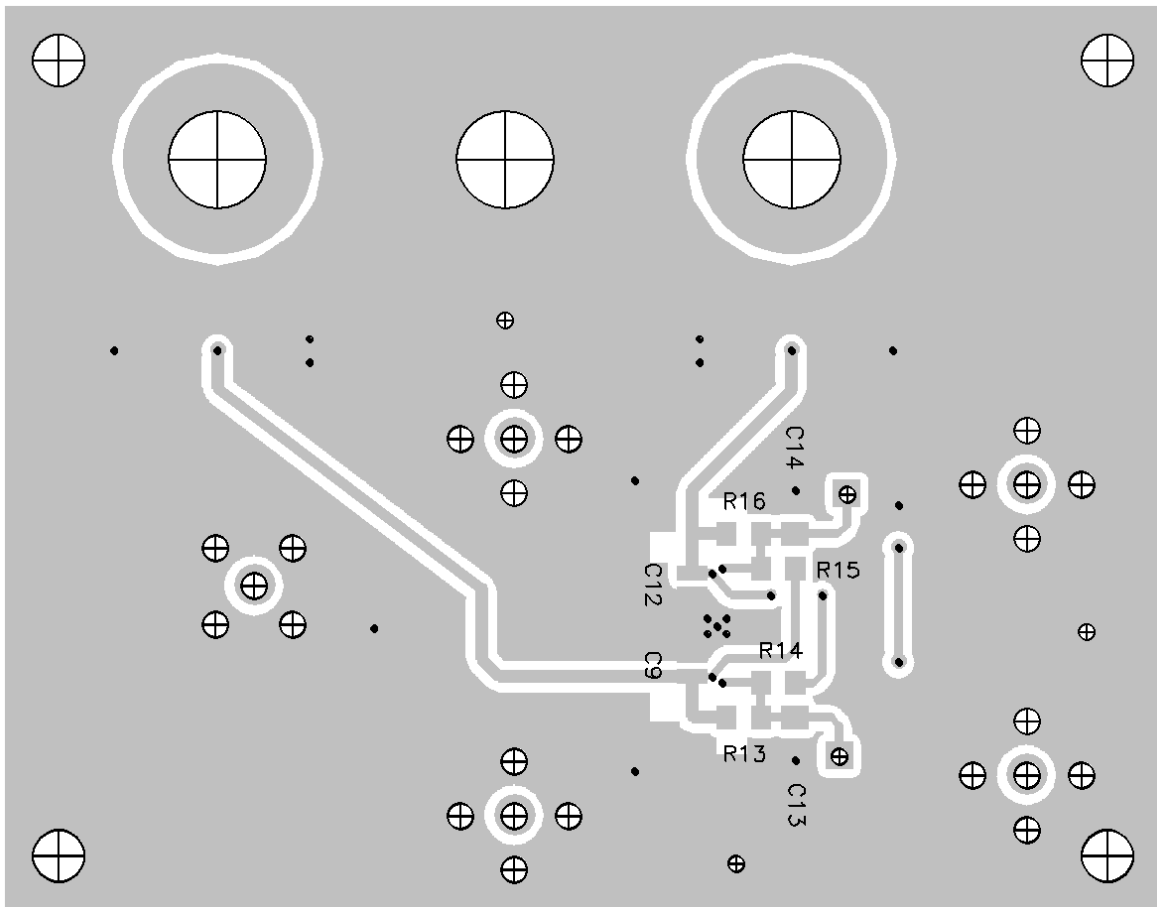
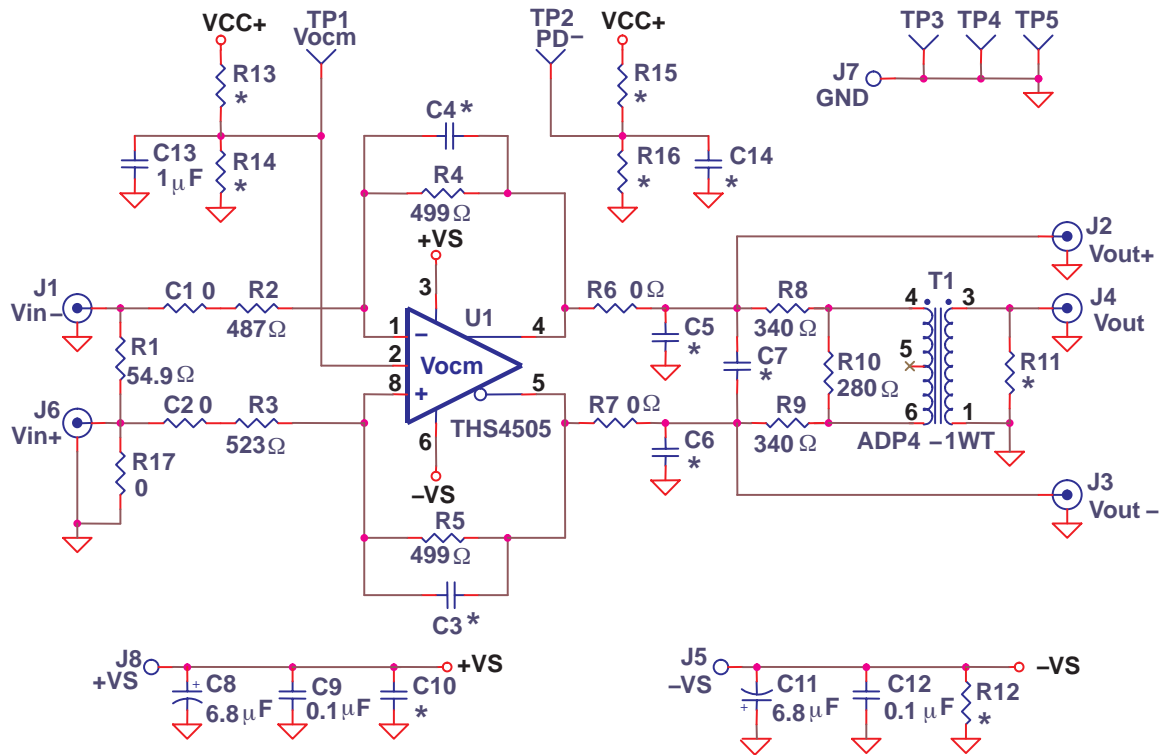


Figure 5–3. Schematic Diagram



**Note:** Devices designated with an \* are not installed on the EVM. The user must supply these components.